

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION**

FENNER INVESTMENT, LTD.	§	
	§	
Plaintiff	§	
	§	
vs.	§	CASE NO. 6:07 CV 8
	§	PATENT CASE
MICROSOFT CORPORATION, NINTENDO COMPANY, LTD., and NINTENDO OF AMERICA, INC.,	§	
	§	
	§	
Defendants	§	

MEMORANDUM OPINION

This opinion construes the terms in U.S. Patent No. 6,297,751 (the “751 patent”).

BACKGROUND

The patent in suit involves a method for interfacing a standard-voltage joystick with a low-voltage port of a processor. The prior art joysticks and integrated circuits both operated using a five volt power supply. However, the next generation of integrated circuits operated on less than five volts, which required a low-power port to interface the traditional joystick and new integrated circuit. The present invention was designed to address this problem.

Fenner Investment, Ltd. (“Fenner”) alleges Microsoft Corporation, Nintendo Company, Ltd., and Nintendo of America, Inc. (collectively “Defendants”) infringe the ’751 patent.

APPLICABLE LAW

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). In claim construction, courts examine the patent’s intrinsic

evidence to define the patented invention's scope. *See id.*; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). This intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id.* Other asserted or unasserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id.* Differences among the claim terms can also assist in understanding a term's meaning. *Id.* For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id.* at 1314–15.

“[C]laims ‘must be read in view of the specification, of which they are a part.’” *Id.* (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). “[T]he specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Id.* (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's lexicography governs.

Id. Also, the specification may resolve ambiguous claim terms “where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone.” *Teleflex, Inc.*, 299 F.3d at 1325. But, “[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.” *Comark Commc’ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc. v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) (“As in the case of the specification, a patent applicant may define a term in prosecuting a patent.”).

Although extrinsic evidence can be useful, it is “less significant than the intrinsic record in determining the legally operative meaning of claim language.” *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id.* at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert’s conclusory, unsupported assertions as to a term’s definition is entirely unhelpful to a court. *Id.* Generally, extrinsic evidence is “less reliable than the patent and its prosecution history in determining how to read claim terms.” *Id.*

ANALYSIS

An interface between a joystick device having a first source voltage and a processor

“An interface between a joystick device having a first source voltage and processor” is the preamble to Claim 1. The parties dispute whether this preamble limits the claim. Defendants contend that the preamble is a limitation because the preamble serves as antecedent basis and the patentee added the term “first source voltage” to traverse a prior art reference. Plaintiff argues that it is not a limitation because the words of the preamble do not limit the structure claimed.

Generally, a preamble limits the invention if it recites essential structure or if it is “necessary to give life, meaning, and vitality” to the claim. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999). Certain guideposts exist to gauge whether a preamble limits the claim; one such guidepost is the dependence on a particular disputed preamble phrase for an antecedent basis. *Catalina Mktg. Int'l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). “When limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention.” *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003).

Claim 1's preamble provides an antecedent basis for the words “interface,” “joystick device,” and “first source voltage.” *See, e.g.*, ‘751 patent, col. 5:24–28 (preamble states “a joystick device” which is the antecedent basis for “the joystick device” used in the body of the claim). Fenner argues that these words do not further limit the structure that is claimed. However, as an example, a limitation of the claim is “an interface circuit having a second source voltage that is lower than the first source voltage.” *Id.* at col. 5:30–31. The phrase “first source voltage” finds antecedent basis only in the preamble. This applies equally to “interface” and “joystick device.” *See id.* at col. 5:24–46. Accordingly, the preamble is a claim limitation; however, as discussed below, the phrase

does not require a separate construction apart from what is in the claim.

An interface interfacing said joystick device with said processor¹

Defendants contend that the phrase should be construed as “a port between a higher voltage joystick and a lower voltage processor that enables communication with the processor.” Fenner claims the phrase needs no construction. The disputes are whether the “interface” should be construed as a “port” and whether this term includes a dual voltage requirement.

Defendants argue that the term “port” and “interface” are synonymous. Fenner claims that the terms are not synonymous. The specification repeatedly refers to the interface as a “port interface.” *See, e.g.*, ‘751 patent, cols. 1:64; 2:14–15, 21–22. However, the patent also uses the word interface without prefacing the term with “port.” *Id.* at col. 2:30–31. The claim language does not include the “port” modifier when claiming the interface. If the patentee had intended to limit the interface to a port, the patentee could have drafted the language to that effect. *See Cordis Corp. v. Medtronic Ave, Inc.*, 511 F.3d 1157, 1174 (Fed. Cir. 2008). Because the patentee claimed “interface” without the “port” modifier, it would be improper to limit “interface” to being a “port.”

Defendants also claim that the dual voltage requirement is a necessary part of the interface. The dual voltage requirement is already a limitation found in the claim language; thus, there is no need to construe “interface” to include those limitations. *See* ‘751 patent, col. 6:26–27 (“an interface circuit having a second source voltage that is lower than the first source voltage”). Accordingly, as the Court has resolved the parties’ disputes, there is no need to construe this phrase.²

¹ The parties agree that the phrases “an interface between a joystick device having a first source voltage and a processor” in Claim 1 and “interfacing a joystick device having a first source voltage with a processor” in Claim 14 are substantially similar to this phrase, which is in Claim 9. Thus, the Court’s analysis of the language in Claim 9 applies with equal weight to the language in Claim 1 and Claim 14.

² While it is the district court’s duty to resolve the parties’ disputes regarding the scope of a claim term, this does not require the court to construe every limitation present in the claim. *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

Resistor Capacitor (RC) Network

The Court modifies Defendants' construction and construes "RC network" as "one or more resistors coupled with one or more capacitors to form a circuit having time-based characteristics."

Fenner's proposed construction is "at least one resistor component and at least one capacitor forming a network." Fenner's construction glosses over one of the key terms—"network." As illustrated during the *Markman* hearing, the parties' dispute focuses on the meaning of "network." Fenner's construction does nothing to resolve, or even address, the "network" dispute, which would improperly leave the issue for the jury to resolve. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

Defendants proposed "a resistor coupled with a capacitor to form a circuit having a time constant." Fenner contends this construction limits the term to just one resistor and one capacitor having one time constant. At the *Markman* hearing, the parties agreed that an RC network could consist of multiple resistors and capacitors. *See Markman* Hrg Tr. at 16:8–9, 26:25–27:3.

The sole remaining dispute is over the term "time constant." Fenner argues that the issue of time is not relevant to the construction of RC network. At the hearing, the Court gave each party the opportunity to submit supplemental extrinsic evidence on the issue of time constants. In the supplemental briefing, both sides' experts agreed that RC networks have timing characteristics but disputed the relevance to the present invention. Docket No. 134, Exh. A ¶ 6; Docket No. 135, Exh. A ¶¶ 4 and 19. One of ordinary skill in the art would understand that in the patent the term "network" in RC network denotes timing characteristics. Accordingly, the Court construes "RC network" to mean "one or more resistors coupled with one or more capacitors to form a circuit having time-based characteristics."

Capacitor that generates an analog joystick position measurement signal³

The Court construes this phrase as “a capacitor that generates an analog signal, which is used to indicate the joystick position.”

Fenner’s proposed construction is “a capacitor that generates an analog signal corresponding to a measure of position of the joystick device.” Fenner’s reliance on the word “corresponding” is vague and may tend to confuse the fact finder.

Defendants propose the term means “a capacitor that charges at a rate in direct relation to an analog joystick position to produce a voltage waveform.” Defendants contend that the correct construction flows from their construction of “RC network,” but they improperly attempt to change the claimed function “generates” to “charges at a rate in direct relation to.” Defendants cite no support for the “charges at a rate” language, and nothing in the intrinsic evidence supports importing this limitation.

While the specification does not refer to a charge rate, it does teach that the capacitor generates the joystick position signal while charging. *See* ‘751 patent, cols. 1:40–51; 4:24–37. The patent refers to this analog signal as “JSout.” *Id.* at Fig. 2, col. 1:33–35. JSout is used to determine the joystick position. *See id.* at col. 4:29–37. Thus, one of ordinary skill in the art would understand that the capacitor generates an analog signal (JSout in the ‘751 patent) and uses that signal to indicate the joystick position. Accordingly the Court construes the phrase to mean “a capacitor that generates an analog signal, which is used to indicate the joystick position.”

³ The parties agree that this phrase and the phrase “a capacitor that generates said analog joystick measurement signal” in Claim 14 are substantially similar and warrant the same construction.

Interface circuit⁴

The Court construes “interface circuit” to mean “a circuit that connects the joystick and the processor.”

Fenner proposes the term means “a circuit that receives an analog joystick position measurement signal and outputs a digital signal that corresponds to a position value of the joystick.” Fenner’s construction addresses components of an interface circuit, but it does not define “interface circuit.” For example, Claim 1 states that the buffer circuit receives the joystick position signal and outputs a digital signal. ‘751 patent, col. 5:32–39. The claim then states that the pulse generator generates a pulse based on that digital signal, which the specification defines as a digital pulse signal. *Id.* at cols. 5:40–46, 2:1–2, Abstract. While Fenner’s construction is correct as to the functionality of the interface circuit, parroting the claim language does nothing to clarify the term for the fact finder.

Defendants propose “interface circuit” means “a circuit that enables communications between the joystick and the processor.” Defendants cite no evidence to support the “enables communications” language. The specification teaches that the interface circuit interfaces a joystick peripheral device with a lower power computer port. *Id.* at col. 1:65–67. Figure 2 illustrates the interface circuit, which shows that the joystick connects to the host computer through the interface circuit. *See id.* at Fig. 2, col. 2:21–33. One of ordinary skill in the art would understand that the interface circuit is the connection between the joystick and processor. *See id.* at Fig. 2. Accordingly, the Court construes “interface circuit” as “a circuit that connects the joystick and the processor.”

⁴ Originally the parties asked the Court to construe “interface circuit having a second source voltage that is lower than the first source voltage.” At the *Markman* hearing, the parties agreed that the only disputes were over the terms “interface circuit” and “source voltage.” *Markman* Hr’g Tr. at 41:8–17. Accordingly, the Court only construes those terms.

Source voltage

The Court construes “source voltage” to mean “the source of voltage that provides power to the circuit.”

Fenner’s proposed construction is “the voltage being supplied.” Fenner’s construction reads the word “source” out of the claim, which would allow any signal to satisfy this limitation.

Defendants propose “source voltage” means “a power supply voltage.” Defendants’ construction limits the source voltage to one that is supplied by a power supply, which necessarily excludes other techniques for supplying a source voltage. Nothing in the intrinsic evidence limits the source voltage to only a power supply. Thus, Defendants’ construction is too narrow.

The specification teaches that the invention is designed to interface “a typical 5 volt joystick peripheral device with a lower power computer port.” ‘751 patent, col. 2:65–67. One of ordinary skill in the art would understand that the interface was designed to connect two systems that have different “source voltages.” These different voltage sources would provide the circuit with power. Accordingly, the plain and ordinary meaning of “source voltage” is “the source of voltage that provides power to the circuit.”

Buffer circuit

The Court construes the term as “a circuit that separates the lower voltage circuitry from the higher voltage circuitry.”

Fenner proposes the term means “circuit having an input and an output to receive the analog joystick position measurement signal and convert the signal to a digital signal.” Defendants’ proposed construction is “a circuit generating a digital output that switches logic states (i.e., from logic level 1 to logic level 0 or from logic level 0 to logic level 1) when the analog joystick position measurement signal exceeds a predefined voltage threshold.” Both parties are attempting to include

their versions of limitations found elsewhere in the claim, but neither party defines a buffer circuit, which has an embodiment described as including “a three-state buffer 222 and an input buffer 224.” ‘751 patent, col. 2:34–35.

The specification teaches that the interface includes a pulse generator and a bi-directional buffer circuit. ‘751 patent, cols. 1:67–2:1, 2:32–33. The claim language states that the joystick device has a first source voltage and that the interface circuit has a second source voltage that is lower than the first source voltage. *Id.* at col. 5:24–25, 30–31. The buffer circuit, as the word denotes, acts as a buffer between the higher voltage joystick signal and the lower voltage in the interface circuit. *See id.* at Fig. 2, cols. 1:64–2:4, 5:31–39. One of ordinary skill in the art would understand that the buffer circuit separates the higher voltage joystick circuitry from the lower voltage interface circuitry. Accordingly, the Court construes “buffer circuit” as “a circuit that separates the lower voltage circuitry from the higher voltage circuitry.”

Pulse⁵

The Court construes this term to mean “a single cycle of variation in the logic level of a signal.” The intrinsic evidence does not accord a special definition to “pulse,” so its plain and ordinary meaning applies. *Symantec Corp. v. Computer Assocs. Int’l, Inc.*, 522 F.3d 1279, 1291 (Fed. Cir. 2008). The relevant meaning is as one of ordinary skill in the art at the time of the invention would understand the term, and dictionaries are “among the many tools that can assist the court in determining the meaning of particular terminology to those of skill in the art of the invention.” *Id.* (quoting *Phillips*, 415 F.3d at 1318).

The IEEE Dictionary defines pulse, in relevant part, as “(4) a wave that departs from an

⁵ The parties originally requested the Court construe the phrases “a pulse based on said signal” (Claims 1 and 9) and “a pulse based on the logic level of said first digital signal” (Claim 14). However, at the *Markman* hearing, the parties stated that the real dispute centered around the meaning of “pulse.” Thus, the Court construes that meaning and accords the other words of the phrase their plain and ordinary meaning.

initial level for a limited duration of time and ultimately returns to the original level.” Docket No. 128, Exh. E at 835. The Prentice Hall’s Illustrated Dictionary of Computing similarly defines pulse as “a variation in value of a magnitude, short in relation to the time schedule of interest, the final value being the same as the initial value.” Docket No. 126, Exh. 16 at 547. The claim mentions two logic states, first and second. ‘751 patent, col.5:33–37. Considering the term in the context of the claim language, one of ordinary skill in the art would understand that “pulse” is a variation of the logic level of the signal.

Accordingly, the Court construes the term as “a single cycle of variation in the logic level of a signal.”

Pulse generator

The Court construes this term as “a circuit that produces a digital output representing a joystick coordinate position based upon the output of the buffer circuit.”

Defendants propose “a circuit producing a digital output that switches logic states for a duration of time in direct relation to an analog joystick position.” Defendants’ construction focuses on the term “pulse,” the product of the pulse generator, and not on “pulse generator,” the actual term being construed. Defendants also require the duration of time to be directly related to the joystick position. To support the “direct relation” limitation, Defendants rely on the description of the prior art and the sole preferred embodiment. Docket No. 126 at 16.

The claim language states that the pulse generator generates a pulse based on the digital signal. ‘751 patent, col. 5:40–41. In the Summary of the Invention, the specification teaches that the digital signal “represents a joystick coordinate position, based on an input analog measurement signal.” *Id.* at col. 2:2–4. Neither the claim nor specification support a “direct relation” limitation. Defendants’ attempt to import this limitation from the only preferred embodiment is improper. *See*

Phillips, 415 F.3d at 1323 (“we have expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment”).

Fenner proposes the term means “a circuit that produces a digital output ‘representing a joystick coordinate position, based on an input analog measurement signal.’” The specification teaches that the bidirectional buffer circuit and the pulse generator act together “to generate the digital pulse signal, representing a joystick coordinate position, based on an input analog measurement signal.” ‘751 patent, col. 2:1–4. Fenner’s proposed construction does not distinguish the function of the pulse generator from the function of the buffer circuit; it simply states the combined end result. Thus, the Court modifies Fenner’s construction to read out the buffer circuit portion. Accordingly, the Court construes “pulse generator” as “a circuit that produces a digital output representing a joystick coordinate position based upon the output of the buffer circuit.”

A width of said pulse representing a coordinate position of said joystick device

The Court construes this phrase to mean “the width of the pulse, as assessed in time or distance, represents a coordinate position of the joystick device.”

Defendants’ proposed construction is “the duration of the pulse varies in direct relation to a coordinate position of the joystick.” Fenner contends that Defendants’ construction imports the limitations of time and direct relationship. However, at the *Markman* hearing, both sides agreed that width could be measured in units of time or distance; thus, the sole issue is the “direct relation” limitation. *Markman* Hr’g Tr. at 78:2–21.

Defendants claim the specification teaches that the pulse width is in direct relation with the coordinate position of the joystick. However, support for Defendants’ position is found in the description of the prior art, not the present invention. *See* ‘751 patent, col. 1:45–52. When

describing the present invention, the specification teaches that the digital pulse signal represents a joystick coordinate position not that the pulse is directly related to the joystick position. *Id.* at col. 2:2–3. Thus, Defendants’ “direct relation” limitation is improper.

The parties’ disputes centered around how to measure width and whether a direct relation was necessary. As discussed above, “direct relation” is an improper limitation, and the parties agree that width may be measured in time and distance. As the parties do not dispute the other language of the phrase, the Court construes this phrase as “the width of the pulse, as assessed in time or distance, represents a coordinate position of the joystick device.”

The capacitance value of said capacitor being [is] a function of said predetermined threshold that prevents deviation of the width of said pulse from expected values

The Court adopts Fenner’s construction and construes this phrase as “the value of a capacitor’s ability to hold a charge is selected in relation to the predetermined threshold so that a pulse width of the digital signal conforms to expected values.”

Defendants’ proposal is “the size of the capacitor is calculated from the predetermined voltage threshold used such that the pulse width is no shorter and no longer than predetermined minimum and maximum values.” The parties’ dispute focuses on two areas: the “being a function of” and “prevents deviation . . . from expected values” claim language.

Defendants construe “being a function of” as “calculated from.” At the hearing, Defendants stated that the specification does not require a specific formula to perform the calculation but it does require a mathematical equation be used. However, the only calculations shown in the patent are contained in the preferred embodiment and found as limitations in dependent claims 8, 13, and 19. *See* ‘751 patent, cols. 5:6–13, 6:5–12, 7:1–5, 8:20–25. The specification does not limit “being a function of” to a mathematical formula. It teaches that the capacitance “may be selected in relation to” the predetermined threshold. *Id.* at col. 5:1–3. While this requires the manufacturer or designer

of the accused system to set the threshold in advance, it does not require a calculation be performed.

The parties also dispute the meaning of the “expected values” language. Defendants want to include the limitations of “no shorter or no longer than predetermined minimum and maximum values.” In the single embodiment, the specification teaches:

The pulse width of the PCin signal, which represents the rise time, however, should not be less than or exceed expected minimum/ maximum pulse width values. Therefore, to ensure optimal joystick position sensing, the capacitance (“Cnew”) of the RC network capacitor 124 may be selected in relation to Vtnew.

In other words, Cnew is set so that the pulse width of PCin conforms to expected minimum/ maximum values.

Id. at cols. 4:64–5:4. It is apparent that the “minimum/ maximum” values are a type of expected value. However, the claim language is drafted more broadly and does not confine the term to a certain type of expected values. Given the broad language used in the claim, the description in the embodiment should not limit the claim. *See Liebel-Flarshiem Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (“this court has expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment”).

One of ordinary skill would understand that the capacitance value is the capacitor’s ability to hold a charge. As stated above, the specification teaches that the capacitance “may be selected in relation to” the predetermined threshold. *Id.* at col.5 :1–3. Also, the claim language does not limit the expected values to a specific type. Accordingly, after resolving the parties’ dispute, the Court construes the phrase as “the value of a capacitor’s ability to hold a charge is selected in relation to the predetermined threshold so that a pulse width of the digital signal conforms to expected values.”

Latch

The Court rejects Fenner’s and Defendants’ proposed constructions and construes this term to mean “a circuit that can be used to hold data in a ready position until required.”

Defendants' proposed construction is "a circuit that holds one of two steady logic output levels depending on its inputs." Defendants argue that the specification limits a latch to a D-type flip-flop or similar latch. While the specification does describe a "D-type flip-flop," this description is part of the preferred embodiment. *See '751 patent, col. 2:39–41.* Defendants again are attempting to import limitations found only in a preferred embodiment without support from the claim language, which is improper. *See Phillips, 415 F.3d at 1323; Liesel-Flarshiem, 358 F.3d at 906.*

Fenner proposes the term means "an electronic circuit used to store information." Relying on the IEEE Dictionary, Fenner argues that its construction is the plain and ordinary meaning of "latch." The IEEE Dictionary defines "latch" as "(A) a circuit that can be used to hold data in a ready position until required; usually controlled by another circuit. (B) A circuit consisting of one or more latches as in (A) that is used to store digital data." Docket No. 123, Exh B. Fenner's construction broader than the IEEE's because it could include any generic memory device.

When the intrinsic evidence does not lend a special meaning to a term, a court must accord the term its ordinary and customary meaning. *Symantec Corp. v. Computer Assocs. Int'l, Inc., 522 F.3d 1279, 1291 (Fed. Cir. 2008).* Fenner states that the IEEE definition is the plain and ordinary meaning of the term. Defendants concede that the IEEE definition of "latch" is consistent with Defendants' proposed construction, but Defendants contend that the definition should track the preferred embodiment. As explained above, the claim language does not support importing the embodiment's limitations. Accordingly, the Court accords "latch" its plain and ordinary meaning and construes the term as "a circuit that can be used to hold data in a ready position until required."

CONCLUSION

For the foregoing reasons, the Court interprets the claim language in this case in the manner set forth above. For ease of reference, the Court's claim interpretations are set forth in Appendix B.

The claims with the disputed terms in bold are set forth in Appendix A.

So ORDERED and SIGNED this 22nd day of August, 2008.

A handwritten signature in black ink, appearing to read "LEONARD DAVIS", is written over a horizontal line. The signature is fluid and cursive, with a large loop on the left and a smaller loop on the right.

**LEONARD DAVIS
UNITED STATES DISTRICT JUDGE**

APPENDIX A

1. An interface between a joystick device having a first source voltage and a processor, comprising:
a Resistor-Capacitor (RC) network, connected to the joystick device, said RC network having a capacitor that generates an analog joystick position measurement signal; and
an interface circuit having a second source voltage that is lower than the first source voltage, including
a buffer circuit, in a first operation mode of said interface, receiving said analog joystick position measurement signal, outputting a first logic state as a digital signal before said analog joystick measurement signal exceeds said predetermined threshold, and outputting a second logic state as said digital signal after said analog joystick measurement signal exceeds said predetermined threshold; and
a pulse generator generating a pulse based on said digital signal in said first operation mode of said interface, a width of said pulse representing a coordinate position of said joystick device, the capacitance value of said capacitor being a function of said predetermined threshold that prevents deviation of the width of said pulse from expected values.
3. The interface of claim 1, wherein said buffer circuit is connected to a charge storage device, and places said charge storage device in a discharged state in a second operation mode of said interface.
4. The interface of claim 3, wherein said buffer circuit permits said charge storage device to begin charging in said first operation mode of said interface.
6. The interface of claim 1, wherein said pulse generator is a latch.
7. The interface of claim 6, wherein said latch is cleared at a beginning of said first operation mode of said interface by a control signal from said processor, and said latch stores a logic "1" when said digital signal is said second logic state.
9. A processor based system, comprising:
a processor;
a joystick device having a first source voltage; and
an interface interfacing said joystick device with said processor, said interface including,
a Resistor-Capacitor (RC) network, connected to the joystick device, said RC network having a capacitor that generates an analog joystick position measurement signal; and
an interface circuit having a second source voltage that is lower than the first source voltage, including
a buffer circuit, in a first operation mode of said interface, receiving said analog joystick position measurement signal, outputting a first logic state as a digital signal before said analog joystick measurement signal exceeds said predetermined threshold, and outputting a second logic state as said digital signal after said analog joystick measurement signal exceeds said predetermined threshold, and a pulse generator generating a pulse based on said digital signal in said first operation mode of said interface, a width of said pulse representing a coordinate position of said joystick device, and outputting said pulse to said processor, wherein the capacitance value of said capacitor is a function of said predetermined threshold that prevents deviation of the width of said pulse from expected values.
12. The processor based system of claim 9, wherein said pulse generator is a latch, said latch is cleared at a beginning of said first operation mode of said interface by a control signal from said processor, said interface by a control signal from said processor, and said latch stores a logic "1" when said digital signal is said second logic state.
14. A method of interfacing a joystick device having a first source voltage with a processor, comprising:
 - (a) receiving an analog joystick measurement signal from a Resistor-Capacitor (RC) network connected to the joystick device, said RC network having a capacitor that generates said analog joystick measurement signal;
 - (b) generating a digital signal, the logic level of said digital signal being set based on whether said analog joystick measurement signal exceeds a predetermined threshold level, said digital signal being generated by an interface circuit having a second source voltage that is lower than the first source voltage;

- (c) outputting said digital signal to a **pulse generator**;
- (d) generating a **pulse based on the logic level of said first digital signal, a width of said pulse representing a coordinate position of said joystick device**; and
- (e) outputting said pulse to said processor, wherein the **capacitance value of said capacitor is a function of said predetermined threshold level that prevents deviation of the width of said pulse from expected values**.

APPENDIX B

U.S. Patent No. 6,297,751	
Disputed Claim Terms	Court's Construction
interface between a joystick device having a first source voltage and a processor (Claim 1)	No construction
interface interfacing said joystick device with said processor (Claim 9)	
interfacing a joystick device having a first source voltage with a processor (Claim 14)	
a joystick device having a first source voltage and a processor (Claims 1, 9, and 14)	[AGREED] a peripheral device operating a first power supply voltage and having a control stick that produces an analog output signal indicating position of the control stick
Resistor-Capacitor (RC) Network (Claims 1, 9, and 14)	one or more resistors coupled with one or more capacitors to form a circuit having time-based characteristics
capacitor that generates an analog joystick position measurement signal (Claims 1 and 9)	a capacitor that generates an analog signal, which is used to indicate the joystick position
a capacitor that generates said analog joystick position measurement signal (Claim 14)	a capacitor that generates an analog signal, which is used to indicate the joystick position
interface circuit (Claims 1, 9, and 14)	a circuit that connects the joystick and the processor
source voltage (Claims 1, 9, and 14)	the source of voltage that provides power to the circuit
buffer circuit (Claims 1, 3, 4, and 9)	a circuit that separates the lower voltage circuitry from the higher voltage circuitry
pulse (Claims 1, 9, and 14)	a single cycle of variation in the logic level of a signal
pulse generator (Claims 1, 9, and 14)	a circuit that produces a digital output representing a joystick coordinate position based upon the output of the buffer circuit
a width of said pulse representing a coordinate position of said joystick device (Claims 1, 9, and 14)	the width of the pulse, as assessed in time or distance, represents a coordinate position of the joystick device
the capacitance value of said capacitor being [is] a function of said predetermined threshold that prevents deviation of the width of said pulse from expected values (Claims 1, 9, and 14)	the value of a capacitor's ability to hold a charge is selected in relation to the predetermined threshold so that a pulse width of the digital signal conforms to expected values

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Disputed Claim Terms	Court's Construction
latch (Claims 6 and 7)	a circuit that can be used to hold data in a ready position until required